IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Filippi, et al.	**Conf. No.:**	5696
Serial No.:	10/711,697	**Art. Unit:**	2822
Filed:	9/30/2004	**Examiner:**	Au, Bac H.
Title:	**GAS DIELECTRIC STRUCTURE FORMING METHODS**	**Docket. No.:**	FIS920040188US1 (IBMF-0067)

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

DECLARATION UNDER 37 C.F.R. 1.131

We, the Applicants in the above-identified patent application, declare as follows:

1. That we are the inventors of the subject matter described and claimed in the above-identified patent application.

2. That prior to January 23, 2004, we conceived of a method of forming a gas dielectric structure for a semiconductor structure, the method comprising the steps of:

forming an opening for semiconductor structure in a dielectric layer on a substrate;

depositing a sacrificial layer over the opening such that the sacrificial layer fails to substantially fill the opening;

performing a directional etch on the sacrificial layer to form a sacrificial layer sidewall on

the opening after depositing the sacrificial layer;

depositing a conductive liner over the opening after performing the directional etch;

depositing a metal in the opening after depositing the conductive liner;

planarizing the metal and the conductive liner after depositing the metal;

removing the sacrificial layer sidewall after the metal and the conductive liner are planarized, forming a void; and

depositing a cap layer over the void to form the gas dielectric structure.

3. That prior to January 23, 2004, we conceived of a method of forming a gas dielectric structure for a semiconductor structure, the method comprising the steps of:

performing a dual damascene process to form an opening including at least one wiring opening and at least one via in a dielectric layer on a substrate;

depositing a sacrificial layer over the opening;

performing a directional etch on the sacrificial layer to form a sacrificial layer sidewall wherein the directional etching removes the sacrificial layer only from substantially horizontal surfaces;

depositing a conductive liner over the opening after performing the directional etch;

depositing a metal in the opening after depositing the conductive liner;

planarizing the metal and the conductive liner after depositing the metal;

removing the sacrificial layer sidewall after the metal and the conductive liner are planarized, forming a void; and

depositing a cap layer over the void to form the gas dielectric structure.

4. That prior to January 23, 2004, we conceived of a method of forming a gas dielectric structure for a semiconductor structure, the method comprising the steps of:

performing a via-first dual damascene process to form an opening including at least one wiring opening and at least one via in a dielectric layer on a substrate;

depositing a sacrificial layer over the opening such that the sacrificial layer fails to substantially fill the opening;

performing a directional etch on the sacrificial layer to form a sacrificial layer sidewall, wherein the directional etching removes the sacrificial layer only from substantially horizontal surfaces;

depositing a conductive liner over the opening after performing the directional etch;

depositing a metal in the opening after depositing the conductive liner;

planarizing the metal and the conductive liner after depositing the metal;

removing the sacrificial layer sidewall after the metal and conductive liner are planarized, forming a void that extends along a side of the at least one via; and

depositing a cap layer over the void to form the gas dielectric structure.

5. That the present invention is described in Disclosure of Invention ("Exhibit A") submitted to the IBM Corporation Patent Department on February 20, 2004, wherein the present invention is specifically described in the "Main Idea for Disclosure FIS 8-2004-0088" ("Exhibit B"), at pages 2-3. Exhibit B comprises a printed form of the document ~~linked to Exhibit A~~ (see Exhibit A, text line 41).

6. That the time and date stamps appearing in Exhibits A and B were automatically generated by IBM Corporation's archival system, and have not been, and can not be, manually input, modified, edited, or changed in any way.

7. That, subsequent to the conception of the invention, and up until the patent application filing date of September 30, 2004, we diligently and actively assisted the IBM Corporation Patent Department in the planning, preparation, review, and filing of the above-identified patent application.

Declarants further state that the above statements made of the declarants' own knowledge are true, and that all statements made on information and belief are believed to be true. Declarant makes the above statements with the knowledge that willful false statements and the like are punishable by fine and/or imprisonment, or both, under § 1001 of Title 18 of the United States Code, and that any such willful false statement may jeopardize the validity of this application or any patent resulting therefrom.

Date: 1/30/07 /Ronald J. Filippi/
Ronald G. Filippi

Date: _____ _____
Roy C. Iggulden

Date: _____ _____
Edward D. Kicwra

Date: 1/30/2007 _____
Ping-Chuan Wang

6. That the time and date stamps appearing in Exhibits A and B were automatically generated by IBM Corporation's archival system, and have not been, and can not be, manually input, modified, edited, or changed in any way.

7. That, subsequent to the conception of the invention, and up until the patent application filing date of September 30, 2004, we diligently and actively assisted the IBM Corporation Patent Department in the planning, preparation, review, and filing of the above-identified patent application.

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Date: _____ _____
Ronald G. Filippi

Date: 1/30/2007 R. C. Iggulden
Roy C. Iggulden

Date: _____ _____
Edward D. Kiewra

Date: _____ _____
Ping-Chuan Wang

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Date: _____

_____
Ronald G. Filippi

Date: _____

_____
Roy C. Iggulden

Date: January 31, 2007

Edward W. Kiewra

Date: _____

_____
Ping-Chuan Wang

Exhibit A

Disclosure FIS 8-2004-0088
Prepared for and/or by an IBM Attorney - IBM Confidential

Created By Roy Igguiden On 01/23/2004 04:08:57 PM EST
Last Modified By Enterprise Agentmgr On 05/12/2004 01:33:05 AM EDT

Required fields are marked with the asterisk (*) and must be filled in to complete the form.

***Title of disclosure (In English)**
Method and structure for airgap formation

Summary

Status	Search Results Received
Final deadline	
Final deadline reason	
* Processing location	Fishkill
* Functional area	[redacted]
Attorney/Patent professional	James Cioffi/Fishkill/IBM
IDT team	[redacted]
Submitted date	02/20/2004 04:48:59 PM EST
* Owning division	[redacted]
Incentive program	
Lab	
* Technology code	1011
PVT score	[redacted]

Inventors with a Blue Pages entry
Inventors: Roy Igguiden/Fishkill/IBM, Edward Klewre/Fishkill/IBM, Ronald Filippi/Fishkill/IBM, Ping-Chuan Wang/Fishkill/IBM

Inventor Name	Inventor Serial	Div/Dept	Inventor Phone	Manager Name
> ✓Igguiden, Roy C.	[redacted]	[redacted]	[redacted]	[redacted]
✓Klewre, Edward W. (Ed)				
✓Filippi, Ronald				
✓Wang, Ping-Chuan				

> denotes primary contact

Inventors without a Blue Pages entry

IDT Selection
Main Idea

To view the main idea for this disclosure, click on this doclink ---> (If you are prompted to enter a server name, please enter D01DB068/01/A/IBM)

***Inventor Questions**

Exhibit B

Main Idea for Disclosure FIS 8-2004-0088
Prepared for and/or by an IBM Attorney - IBM Confidential

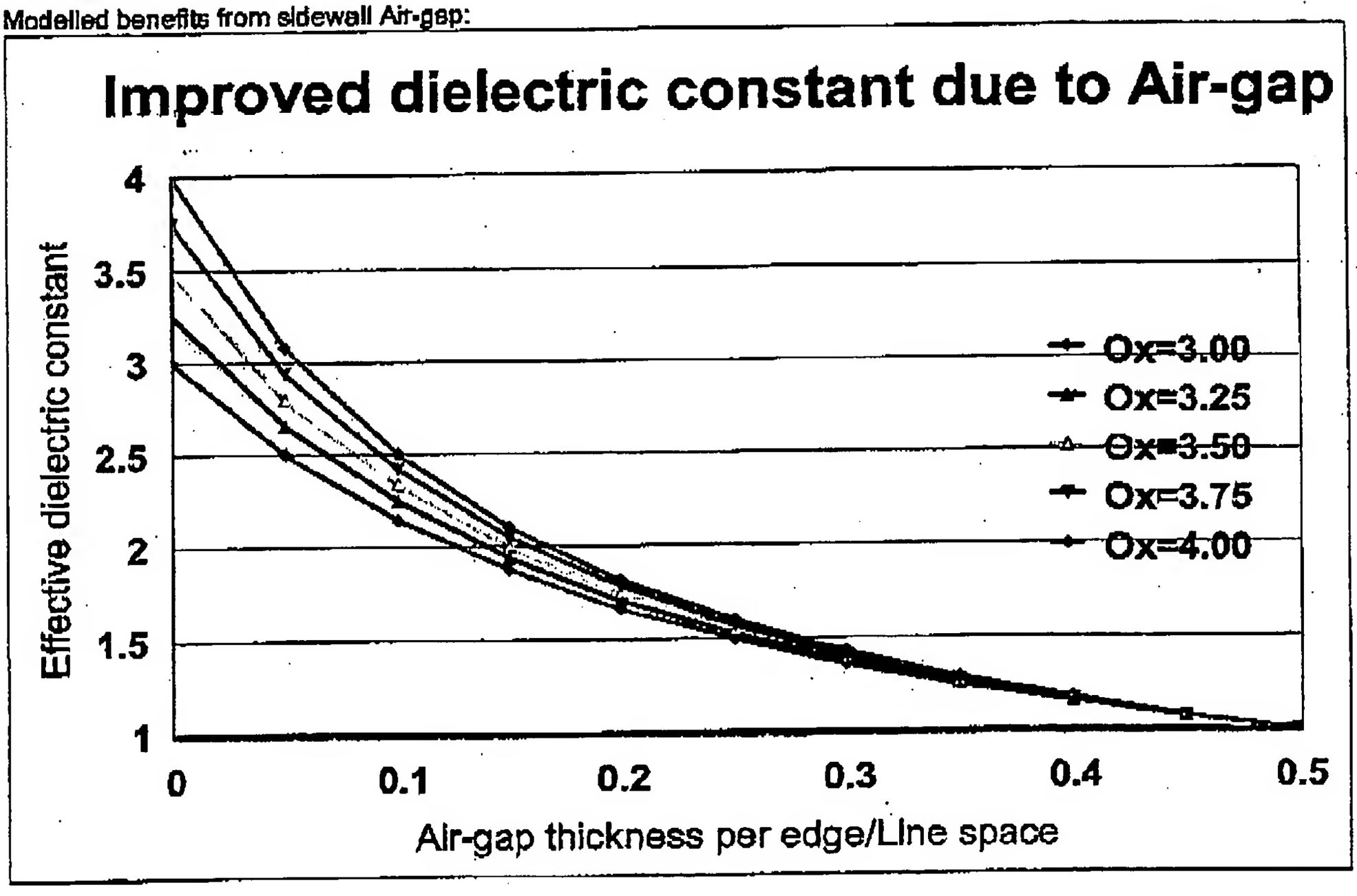
Archived On 03/24/2004 01:02:24 AM

Title of disclosure (in English)
Method and structure for airgap formation

Main Idea

1. Background: What is the problem solved by your invention? Describe known solutions to this problem (if any). What are the drawbacks of such known solutions, or why is an additional solution required? Cite any relevant technical documents or references.
This invention provides capacitance improvement for interconnect devices by using an air gap created by a sacrificial liner material. Capacitance improvements can be also made with low K dielectrics, however our method does not rely on exotic/new material sets. Our invention addresses the formation of a local 'Air-gap' which also reduces the overall BEOL capacitance. Simple capacitance modelling of parallel wires shows that even a small air-gap near the wire results in a vast improvement in the overall K for the structure (ex: a 10% air-gap per edge will reduce the effective dielectric constant of an oxide dielectric from 4.0 to 2.5). Others have created air-gap structures for low K BEOL, however our idea is unique in that it is easily integrated into damescene wire formation, where prior art addresses RIE based structures.

Modelled benefits from sidewall Air-gap:



2. Summary of invention: Briefly describe the core idea of your invention (saving the details for questions #3 below). Describe the advantage(s) of using your invention instead of the known solutions described above.
Advantages:
+ Reduced BEOL capacitance
+ Easily integratable
+ Mechanically stable
+ Requires no new masking levels

3. Description: Describe how your invention works, and how it could be implemented, using text, diagrams and flow charts as appropriate.

Process flow FIGURES: Spacer_Air_Gap.PRZ

All reference to figures refer to the figures contained in the above file. Figures are labeled according to page number.

One process flow which illustrates the concept of our invention is contained in the following text. Starting on any normal substrate, said layer 100, with any normal conductor line, active area, etc patterned in substrate, said layer 110, deposit an ILD, said layer 120. A hard mask layer can be added on top of ILD, said layer 130 (see fig. 1). Said layer 120 can be any of numerous ILD's including but not limited to oxide, fluorinated oxide, SiLK, SICOH, black diamond, etc. Said layer 130 can be any of numerous hard masks including but not limited to oxide, nitride, oxynitride, blok, n-blok, etc. Next, lines and vias are patterned into the said 120 and 130 layers by any standard dual damascene processing (note this invention could also be done in single damascene processing or in metal RIE as well). Figure 2 illustrates the dual damascene patterning. A first liner, said layer 140, is deposited into the previously patterned dual damascene features as shown in Figure 3. This liner can be any of numerous liner materials including but not limited to tantalum (Ta), tantalum nitride (TaN), titanium (Ti), titanium nitride (TiN), tungsten (W), Nb, etc. A sacrifical layer, said layer 150, is deposited on top of liner layer 140 as shown in Figure 4. This sacrificial layer can be any of numerous materials including but not limited to aluminum (Al), oxide, Ti, etc. A directional etch is then done on the said sacrificial layer 150 to form a sidewall layer, said layer 160, as shown in Figure 5. This leaves the sacrifical layer on the sidewalls of the vias and lines but removes it from the bottom of the vias and lines. Next an additional liner(s), said layer 170, is deposited followed by a metal layer, said layer 180, as shown in Figure 6. Said liner 170 can be any material as mentioned for said liner 140. Said metal layer 180 can be any of numerous metal layers including but not limited to copper (Cu), Al, gold (Au), silver (Ag), or alloys there of. Said layers 140, 170 and 180 are polished back by chemical mechanical polishing to form patterned dual damascene structures as shown in Figure 6. Now said sidewall/sacrifical layer 160 is now removed by a wet or dry selective etch from the metal line's sides as shown in Figure 7 to form air gap, said layer 190. A cap, said layer 200, is then deposited on top of the overall structure so that cap does not go to far into air gap as shown in Figure 8. This structure can, of course, be used for any subsequent layers as well.

Additionally, Figure 9 shows that the process could also work without aforementioned liner layer 140 where sacrificial layer is deposited next to ILD. Also, Figure 10 illustrates that in a via first dual damascene application said air gap 190 has the opportunity to go down into one side of the via as well.

The following table shows some materials that can be used as the sacrifical layer and what chemical may be used to etch them that would be selective to the other contact points.

Sacrificial Layer	ILD	Etchant	
Al	oxide	H2O + NaOH (10:1)	
Al	oxide	H2O + HCl (1:1)	
oxide	low k material	H2O + HF (1:1)	

Main Idea for Disclosure FIS8-2004-0088 - continued

oxide	low k material	HF +HCl (1:1)	
[redacted]			